

ABSTRACT

According to one aspect of the present invention, there is provided a semiconductor device comprising a plurality of memory cells, and an error-correction circuit, wherein write operation is performed by a late-write method, and ECC processing is executed in parallel with writing, and thereby cycle time is shortened. Moreover, it is better that when a memory cell is power supplied through a well tap, the same address is not assigned while the memory cell is power supplied through the well tap.